ABSTRACT OF THE DISCLOSURE

There is disclosed a semiconductor memory device which comprises a plurality of bit line pairs each having first and second bit lines arranged in a first direction, a cell array having a plurality of SRAM cells each of which is connected between the first and second bit lines of a corresponding bit line pair via first and second storage nodes, respectively, a plurality of word lines arranged in a second direction crossing the first direction, and a data write circuit which, in the write mode, writes data into an SRAM cell selected by a word line via the first and second bit lines and, in the read mode, rewrites data read onto the first bit line from an SRAM cell selected by a word line onto the first bit line.